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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/753,616	01/04/2001	Hitoshi Asada	001694	1580

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EXAMINER
GEBREMARIAM, SAMUEL A

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 10/29/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/753,616	ASADA ET AL.	
	Examiner	Art Unit	
	Samuel A Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 August 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1, is rejected under 35 U.S.C. 103(a) as being unpatentable over Drowely in view of Gotou US patent No. 5,264,721.

Regarding claim 1, Drowley teaches (fig. 7) a CMOS image sensor comprising; a photodiode having an impurity region having source and drain regions formed respectively in a semiconductor substrate (11), and first (32) and second (31) MOS transistors formed by introducing impurities into the semiconductor substrate, where a silicide film is not formed on a surface of an impurity region of the first MOS transistor having the impurity region connected to the of the photodiode, the first MOS transistor being positioned at least on one side of the photodiode, and a silicide film (44) is formed on a surface of the MOS transistor.

Drowely also teaches (col. 4, line 38-41) forming interlayer dielectric (not shown) over the sensor (10) and making contact to appropriate portions of the device.

Drowley does not explicitly teach an insulating film formed on the first and second MOS transistors, the insulating film having contact holes reaching the source regions and drain regions of the first and second MOS transistors.

It is conventional and also taught by Gotou (figs 7e and 7f) forming an insulating film (21) on a transistor where contact holes are formed in the insulating film in order to expose the source region (6") and drain region (7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the contact holes formed on the insulating layer in the structure of Drowley in order to make contact to the source and drain regions during further metallization.

Claims 2, 3, 5 and 6, are rejected under 35 U.S.C. 103(a) as being unpatentable over Drowely in view of Gotou and in further view of Park US patent No. 6,040,593.

Regarding claim 2, Drowley teaches substantially the entire claimed structure of claim 1 above except stating the first MOS transistor having an impurity region as drain connected to the impurity region of the photodiode, a second MOS transistor having an impurity region as source connected to a source of the first MOS transistor and a third MOS transistor formed on the substrate, the third transistor having an impurity region as a source connected to drain of the second MOS transistor and a silicide film is formed on the surface of source and drain of the third MOS transistor.

It is conventional and also taught by Park (fig. 3) that the CMOS image sensor device comprising more than two MOS transistors.

Drowely teaches the source of the first MOS transistor connected to the impurity region of the photodiode. However it is known in the art the source/drain regions have identical structures and are interchangeable depending on the application.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching from Park in to the structure of Drowely in order to make a CMOS image sensor with more than two transistors as taught by Park.

Regarding claim 3, Drowley teaches (Park fig. 3) substantially the entire claimed structure of claims 1 and 2 above including MOS transistor circuit for processing a signal output from the MOS transistor is formed on the semiconductor substrate.

Regarding claim 5, Drowley teaches substantially the entire claimed structure of claims 1 and 2 above except specifically stating that an interlayer insulating film for covering the first to third MOS transistors, a wiring formed on the interlayer insulating film and a connection plug connecting the wiring to at least one of the sources and the drains of the first, second and third MOS transistors electrically.

It is conventional and also taught by Gotou (figs 7e and 7f) forming an insulating film on a transistor and forming a wiring on the insulating layer and make connection to source and drain regions.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching from Gotou in to the structure of Drowley in order to make connection to other part of the integrated circuit.

Regarding claim 6, Drowley teaches (Park, fig. 3) substantially the entire claimed structure of claims 1 and 2 above including that the drain of the first MOS transistor has no LDD structure and the source/drain of the second MOS transistor and the

source/drain of the third MOS transistor and the drain of the first MOS transistor has LDD structure.

Claim 4, is rejected under 35 U.S.C. 103(a) as being unpatentable over Drowely and Gotou in view of Park.

Regarding claim 4, Drowley and Park both teach substantially the entire claimed structure of claim 1 and 2 above except specifically stating that a timing circuit for supplying a signal to each gate of the first and third MOS transistors at a predetermined timing is provided on the substrate and a reading-out circuit for reading out a signal output from the third MOS transistor is provided on the semiconductor substrate.

It is conventional to provide a timing circuit to a transistor.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a timing circuit for supplying signal and a reading-out circuit as claimed above since without these elements the MOS transistor would not be of much use.

Response to Arguments

2. Applicant's arguments with respect to claims 1-6 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

3. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel Admassu Gebremariam whose telephone number is 703 305 1913. The examiner can normally be reached on 8:00am-4: 30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 305-7646. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Tom Thomas

Samuel Admassu Gebremariam
October 24, 2002

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800